REMARKS

The Examiner is invited to telephone the undersigned to help expedite any further prosecution of the present application.

The Commissioner is hereby authorized to credit any overpayment or to charge any fees or fee deficiencies under 37 C.F.R. §§ 1.16 and 1.17 in connection with this communication to our Deposit Account No. 02-2666.

Respectfully submitted,

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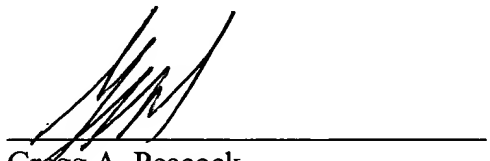

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

[[0001]] [0044] As illustrated in Figure 7, computer system 700 comprises processor 702 that may include instructions for message accumulation and retrieval, as described herein. Computer system also can include another processor 704 that may also have instructions for message accumulation and retrieval, as described herein. Computer system 700 also includes processor bus 710, and chipset 720. Processors 702 and 704 and chipset 720 are coupled to processor bus 710. Processors 702 and 704 may each comprise any suitable processor architecture and for one embodiment comprise an Intel® Architecture used, for example, in the Pentium® family of processors available from Intel® Corporation of Santa Clara, California. Computer system 700 for other embodiments may comprise one, three, or more processors any of which may execute a set of instructions that are in accordance with embodiments of the present invention.

[[0002]] [0045] Chipset 720 for one embodiment comprises memory controller hub (MCH) 730, input/output (I/O) controller hub (ICH) 740, and firmware hub (FWH) 770. MCH 730, ICH 740, and FWH 770 may each comprise any suitable circuitry and for one embodiment is each formed as a separate integrated circuit chip. Chipset 720 for other embodiments may comprise any suitable one or more integrated circuit devices.

[[0003]] [0046] MCH 730 may comprise any suitable interface controllers to provide for any suitable communication link to processor bus 710 and/or to any suitable device or component in communication with MCH 730. MCH 730 for one embodiment provides suitable arbitration, buffering, and coherency management for each interface.

[[0004]] [0047] MCH 730 is coupled to processor bus 710 and provides an interface to processors 702 and 704 over processor bus 710. Processor 702 and/or processor 704 may alternatively be combined with MCH 730 to form a single chip. MCH 730 for one embodiment also provides an interface to a main memory 732 and a graphics controller 734

each coupled to MCH 730. Main memory 732 stores data and/or instructions, for example, for computer system 700 and may comprise any suitable memory, such as a dynamic random access memory (DRAM) for example. Graphics controller 734 controls the display of information on a suitable display 736, such as a cathode ray tube (CRT) or liquid crystal display (LCD) for example, coupled to graphics controller 734. MCH 730 for one embodiment interfaces with graphics controller 734 through an accelerated graphics port (AGP). Graphics controller 734 for one embodiment may alternatively be combined with MCH 730 to form a single chip.

[[0005]] [0048] MCH 730 is also coupled to ICH 740 to provide access to ICH 740 through a hub interface. ICH 740 provides an interface to I/O devices or peripheral components for computer system 700. ICH 740 may comprise any suitable interface controllers to provide for any suitable communication link to MCH 730 and/or to any suitable device or component in communication with ICH 740. ICH 740 for one embodiment provides suitable arbitration and buffering for each interface.

[[0006]] [0049] For one embodiment, ICH 740 provides an interface to one or more suitable integrated drive electronics (IDE) drives 742, such as a hard disk drive (HDD) or compact disc read only memory (CD ROM) drive for example, to store data and/or instructions for example, one or more suitable universal serial bus (USB) devices through one or more USB ports 744, an audio coder/decoder (codec) 746, and a modem codec 748. ICH 740 for one embodiment also provides an interface through a super I/O controller 750 to a keyboard 751, a mouse 752, one or more suitable devices, such as a printer for example, through one or more parallel ports 753, one or more suitable devices through one or more serial ports 754, and a floppy disk drive 755. ICH 740 for one embodiment further provides an interface to one or more suitable peripheral component interconnect (PCI) devices coupled to ICH 740 through one or more PCI slots 762 on a PCI bus and an interface to one or more suitable industry standard architecture (ISA) devices coupled to ICH 740 by the PCI bus

through an ISA bridge 764. ISA bridge 764 interfaces with one or more ISA devices through one or more ISA slots 766 on an ISA bus.

[[0007]] [0050] ICH 740 is also coupled to FWH 770 to provide an interface to FWH 770. FWH 770 may comprise any suitable interface controller to provide for any suitable communication link to ICH 740. FWH 770 for one embodiment may share at least a portion of the interface between ICH 740 and super I/O controller 750. FWH 770 comprises a basic input/output system (BIOS) memory 772 to store suitable system and/or video BIOS software. BIOS memory 772 may comprise any suitable non-volatile memory, such as a flash memory for example.

[[0008]] [0051] Accordingly, computer system 700 includes a machine-readable medium on which is stored a set of instructions (i.e., software) embodying any one, or all, of the methodologies described above. For example, software can reside, completely or at least partially, within main memory 732 and/or within processors 702/704. For the purposes of this specification, the term " machine-readable medium" shall be taken to include any mechanism that provides (i.e., stores and/or transmits) information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.

[[0044]] [0052] Thus, a method and apparatus for initializing a flash memory for the storage of data therein have been described. Although the present invention has been described with reference to specific exemplary embodiments, it will be evident that various modifications and changes may be made to these embodiments without departing from the broader spirit and scope of the invention. For example, data may be stored into Flash memory 104 in sizes other than 16-bits at a time. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

IN THE CLAIMS

5. A method comprising:

receiving a request from an external device to store data into a flash memory of a device, wherein the request includes the size of the data;

initializing the flash memory of the device prior to receiving the data, wherein the initializing comprises[,] :

determining whether the size of free space within the flash memory is greater than the size of the data; and

upon determining that the size of the free space within the flash memory is not greater than the size of the data, reclaiming space within the flash memory. [;

generating headers for each of a number of different locations within the flash memory where the free space is located;

storing the headers into the number of different locations within the flash memory; and

storing pointers, in a separate memory, to the number of different locations within the flash memory where the free space is located;

transmitting a signal to the external device to transmit the data after the initialization of the flash memory is completed;

receiving the data into a number of buffers within the device; and

storing the data within the number of buffers into the number of different locations within the flash memory where the free space is located.]

6. The method of claim 5, further comprising: [wherein the separate memory is a random access memory.]

generating headers for each of a number of different locations within the flash memory where the free space is located;

storing the headers into the number of different locations within the flash memory;

storing pointers, in a separate memory, to the number of different locations within the flash memory where the free space is located;

transmitting a signal to the external device to transmit the data after the initialization of the flash memory is completed;

receiving the data into a number of buffers within the device; and

storing the data within the number of buffers into the number of different locations within the flash memory where the free space is located.

7. The method of claim [5] 6, wherein the device is a cellular telephone and the external device is a server coupled to a network and wherein the data is transmitted to the cellular telephone through a wireless transmission link.

8. The method of claim [5] 6, further comprising disabling interrupts within the device when portions of the data are being written into the number of different locations in the flash memory.

16. The system of claim [1] 14, further comprising storing the data received from the download into a number of buffers prior to storing the data into the flash memory.

17. The system of claim [1] 14, wherein the initialization of the flash memory comprises reclaiming space within the flash memory that is reclaimable for storage of data into the flash memory.